

KKA8133A

DUAL +5.1V +8V REGULATOR WITH DISABLE AND RESET

The KKA8133A is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1 V and 8 V at currents up to 0.75 A. An internal reset circuit generates a reset pulse when the output 1 decreases below the regulated voltage value. Output 2 can be disabled by TTL input.

- Output currents up to 0.75 A
- Fixed precision OUTPUT 1 voltage 5.1 V ± 2%
- Fixed precision OUTPUT 2 voltage 8 V ± 2%
- OUTPUT 1 with RESET facility
- OUTPUT 2 with DISABLE by TTL input
- Short circuit protection at both outputs
- Thermal protection
- Low drop output voltage



**TO-220AB/7
HEPTAWAT**

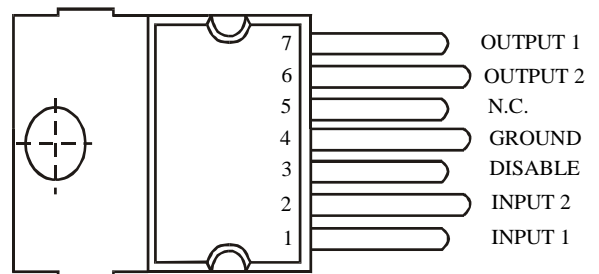
ORDERING INFORMATION

KKA8133A Plastic Package

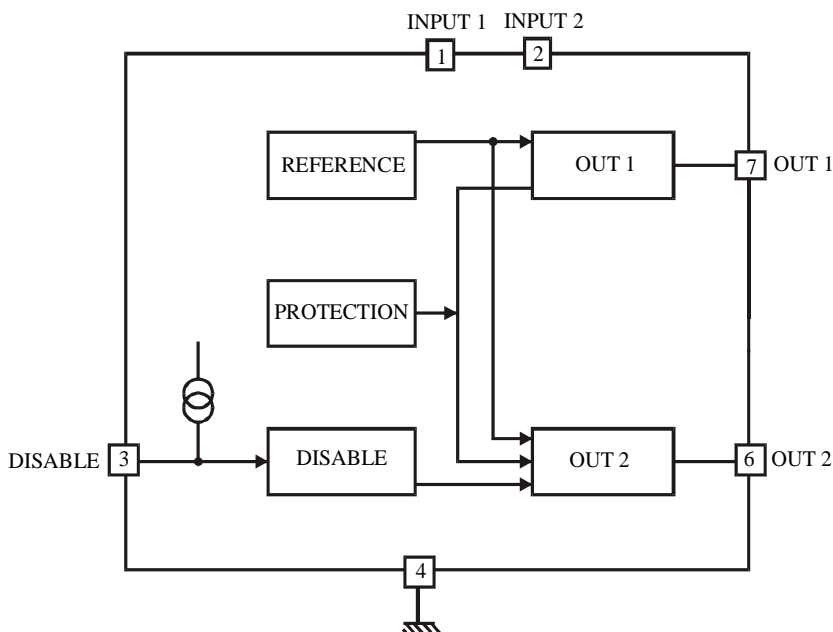
KK8133A chip

$T_j = -0^\circ$ to 130°C

PIN ASSIGNMENT



BLOCK DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{IN1}	DC Input Voltage Pin 1		20	V
V_{IN2}	DC Input Voltage Pin 2		20	V
V_{DIS}	Disable Input Voltage Pin 3		20	V
$I_{O1,2 SC}$	Short Circuit Output Current	$V_{IN1} = 7\text{ V}, V_{IN2} = 10\text{ V}$	1.6	A
		$V_{IN1} = V_{IN2} = 16\text{ V}$	1.0	
Tstg	Storage Temperature	-65	150	°C
T_J	Junction Temperature	0	150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

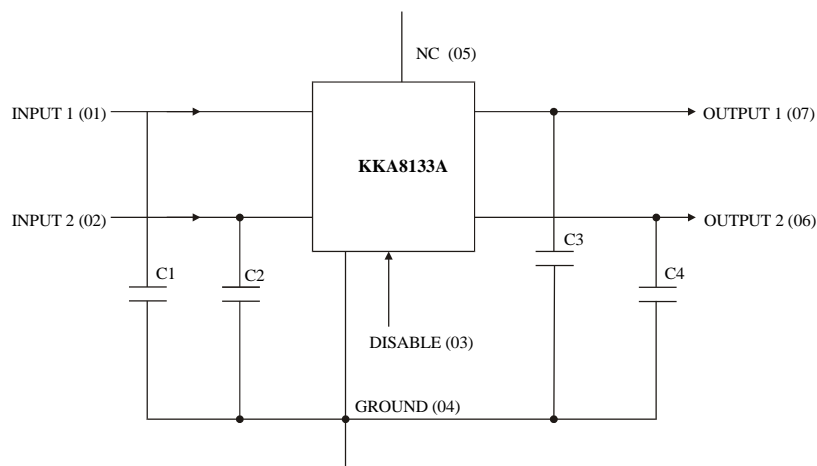
Symbol	Parameter	Min	Max	Unit
V_{IN1}	DC Input Voltage Pin 1	7.0	14	V
V_{IN2}	DC Input Voltage Pin 2	10	14	V
V_{DIS}	Disable Input Voltage Pin 3	0	7.0	V
$I_{O1,2}$	Output Currents		1.0	A
T_J	Junction Temperature	0	130	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
Rth (j-c)	Maximum Thermal Resistance Junction-case	6	°C/W
Rth (j-a)	Maximum Thermal Resistance Junction-ambient	60	°C/W

ELECTRICAL CHARACTERISTICS ($V_{IN1} = 7\text{ V}$, $V_{IN2} = 10\text{ V}$, $T_J = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit
			Min	Max	
V_{O1}	Output Voltage	$V_{IN1} = 7\text{ V}$, $V_{IN2} = 10\text{ V}$, $V_{DIS} = 2.0\text{ V}$, $I_{O1} = -10\text{ mA}$	5.0	5.2	V
		$7\text{ V} \leq V_{IN2} \leq 14\text{ V}$, $-5\text{ mA} \leq I_{O1} \leq -750\text{ mA}$, $V_{DIS} = 2.0\text{ V}$	4.9	5.3	
V_{O2}	Output Voltage	$V_{IN1} = 7\text{ V}$, $V_{IN2} = 10\text{ V}$, $I_{O2} = -10\text{ mA}$	7.84	8.16	V
		$10\text{ V} \leq V_{IN2} \leq 14\text{ V}$, $-5\text{ mA} \leq I_{O1} \leq -750\text{ mA}$, $V_{DIS} = 2.0\text{ V}$, $V_{IN1} = 7\text{ V}$	7.7	8.3	
ΔV_{O1LI}	Line Regulation	$7\text{ V} \leq V_{IN2} \leq 14\text{ V}$, $I_{O1} = -200\text{ mA}$, $V_{DIS} = 2.0\text{ V}$, $V_{IN2} = 10\text{ V}$		50	mV
ΔV_{O2LI}		$10\text{ V} \leq V_{IN2} \leq 14\text{ V}$, $I_{O2} = -200\text{ mA}$, $V_{DIS} = 2.0\text{ V}$, $V_{IN1} = 7\text{ V}$		80	
ΔV_{O1LO}	Load Regulation	$V_{IN1} = 7\text{ V}$, $V_{IN2} = 10\text{ V}$, - $5\text{ mA} \leq I_{O1} \leq -0.6\text{ mA}$, $V_{DIS} = 2.0\text{ V}$		100	mV
ΔV_{O2LO}		$V_{IN1} = 7\text{ V}$, $V_{IN2} = 10\text{ V}$, $-5\text{ mA} \leq I_{O2} \leq -0.6\text{ mA}$, $V_{DIS} = 2.0\text{ V}$		160	
$V_{IO1,2}$	Dropout Voltage	$I_{O1,2} = -750\text{ mA}$, $V_{DIS} = 2.0\text{ V}$		1.4	V
		$I_{O1,2} = -1.0\text{ mA}$, $V_{DIS} = 2.0\text{ V}$		2.0	
I_Q	Quiescent Current	$V_{IN1} = 7\text{ V}$, $V_{IN2} = 10\text{ V}$, $V_{DIS} = 0.8\text{ V}$, $I_{O1} = -10\text{ mA}$		2.0	mA
I_{DIS}	Disable Bias Current	$0\text{ V} \leq V_{DIS} \leq 7\text{ V}$, $V_{IN1} = 7\text{ V}$, $V_{IN2} = 10\text{ V}$	-100	2.0	μA
V_{DISH}	Disable Voltage High (out 2 active)	$V_{IN1} = 7\text{ V}$, $V_{IN2} = 14\text{ V}$	2		V
V_{DISL}	Disable Voltage Low (out 2 disabled)	$V_{IN1} = 7\text{ V}$, $V_{IN2} = 14\text{ V}$		0.8	V

TYPICAL APPLICATION


C1 to C4 = 10 Mf

TO-220 AB/7

